IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND-ODESSA DIVISION

REDSTONE LOGICS LLC,

Plaintiff,

v.

NXP USA, Inc.,

Defendant.

Case No. 7:24-cv-00028-DC-DTG

JURY TRIAL DEMANDED

DEFENDANT NXP USA, INC.'S REPLY CLAIM CONSTRUCTION BRIEF

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B	ON Semiconductor's application note AND8248/D (*Stys*)
C	U.S. Patent No. 7,538,625 (*Cesky*)
D	U.S. Pat. App. Pub. No. 2009/0106576 (*Jacobowitz*)
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I. INTRODUCTION

After originally urging an unbounded "plain and ordinary meaning" construction for the independent clock term, Plaintiff Redstone Logics LLC ("Plaintiff") has pivoted to a construction that is not consistent with plain and ordinary meaning—either in a technical or common English sense—and not consistent with the intrinsic record. By contrast, Defendant NXP USA, Inc.'s ("Defendant") Opening Claim Construction Brief (Dkt. 39 or "Op. Br.") is consistent with the '339 Patent's disclosure and file history, as well as the understanding of a POSITA. Plaintiff's strained characterizations of the file history and specification in its Responsive Claim Construction Brief (Dkt. 41 or "Resp.") merely underscore the uncertain nature of the claims as drafted and the need for the construction sought herein.

II. DISPUTED TERMS REQUIRING CONSTRUCTION

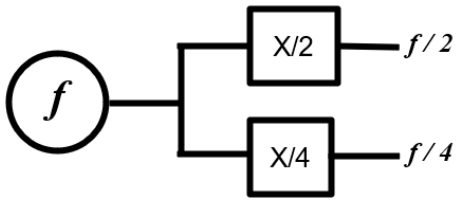
A. Term 1: "the first clock signal is independent from the second clock signal"

Plaintiff has finally shared its purported plain and ordinary meaning of "independent." Plaintiff's position is that "the first clock signal is ***independent*** from the second clock signal" means that "the first clock signal is ***different*** from the second clock signal." Resp. at 2. Plaintiff's position should be rejected because: (a) "independent"—the word the applicant chose to add to the claims and rely on to overcome prior art—is narrower and not the same as "different" both from a technical and plain English sense; and (b) merely "different" clock signals is not consistent with the prosecution history and how the applicant distinguished and overcame prior art of record.

First, it is axiomatic that two clock signals may be "different" but not "independent," which confirms that Plaintiff's plain and ordinary meaning of "independent" is wrong. As Defendant explained in its Opening Brief—and Plaintiff does not address let alone dispute—a device may use a single reference oscillator to generate two different, but dependent clock signals. Op. Br. at 1, 5–6 (discussing *Jacobowitz's* single master reference oscillator and *Kim's* clock distribution

network with a single reference oscillator clock source have multiple different but not independent clock signals).

A simple example confirms that the plain and ordinary meaning of "independent" is not, as Plaintiff argues, "different." A device may have a single reference oscillator and two clock dividers that generate clock signals at one-half and one-fourth times the frequency of the reference oscillator, i.e., clock signals of frequency *f/2* and *f/4* as shown below:



Clock signals at *f/2* and *f/4* ***do not*** meet the plain and ordinary meaning of "independent" because they are dependent on the same input *f*. Yet, *f/2* and *f/4* are plainly different. This confirms that Plaintiff's attempt to replace "independent" with "different" must be rejected as it does not reflect the plain and ordinary meaning of "independent"—and, in view of Plaintiff's stated intent to rewrite the claim under the guise of "plain and ordinary meaning," construction is necessary.

Second, the plain and ordinary meaning of "independent" in the '339 Patent claims cannot be "different" because such a meaning is inconsistent with the intrinsic record. When faced with an obviousness rejection based on the combination of *Jacobowitz* and *Kim*, the applicant chose to amend the claims and chose to use the word "independent," not "different," in those claims. Dkt. 39-9 (Ex. H) at 3–7 (Applicant's Resp. (Nov. 29, 2012)). Likewise, the applicant chose to use the word "independent," not "different," on ***eleven*** occasions in distinguishing *Jacobowitz*, *Kim*, and the combination thereof. *Id.* at 9–11.

Not only did the applicant choose to use "independent" rather than "different," that choice was necessary to distinguish and ultimately overcome what *Kim* disclosed in the context of a

Jacobwitz-Kim combination. Like the example above, *Kim* discloses a single reference oscillator that is used to generate multiple clocks at different frequencies. Specifically, *Kim* discloses a ***single*** clock source 270 that feeds a "main PLL 260," which includes "one ***or more frequency dividers***" to generate multiple ***different*** clock signals as shown in the four colored lines below:

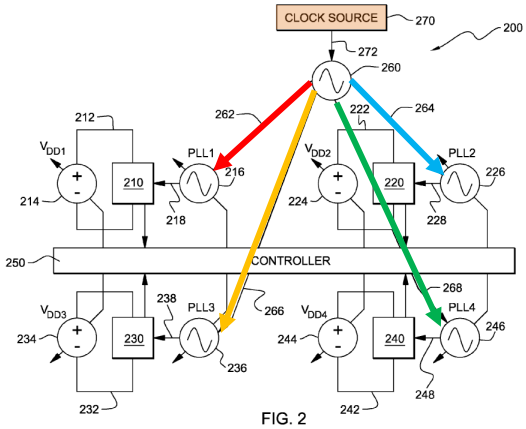


FIG. 2

Dkt. 39-6 (Ex. E) (*Kim*) at Fig. 2 (annotated), [0024]–[0025]; Dkt. 39-1 (Declaration of Dr. Villasenor or "Villasenor Decl.") at ¶¶ 52–53.[1] As with the example above, clock signals 262, 264, 266, and 268 are ***different***, but they are not ***independent*** because they all are multiples of the same original frequency from clock source 270. *Id.* That is, a change to the frequency of clock source 270 will impact each of clock signals 262, 264, 266, and 268. *Id.* ¶¶ 51–52.

Plaintiff argues incorrectly that, "[a]s to Kim, the applicant did not even argue independence of the signals was distinguishing, merely acknowledging it as a limitation." Resp. at 5. The applicant specifically contrasted the claimed independent clocks, explaining that *Kim* instead disclosed a singled sourced clock:

> In addition, the ***first clock signal is independent from the second clock signal. Instead, Kim discloses*** the apparatus comprising a multi-core processor (i.e., 100 in FIG. 1 or 200 in FIG. 2) having ***a single clock source*** (i.e., 170 in FIG. 1 or 270 in FIG. 2). The clock signal from this single clock source is then ***processed (i.e.,***

[1] All emphases added unless otherwise noted.

> ***divided or multiplied)*** and provided to each of the cores. <u>See</u> *Kim* at ¶¶ [0024]-[0025] and FIGs 1 - 2.

See Dkt. 39-9 (Ex. H) at 10–11 (Applicant's Resp. (Nov. 29, 2012)) (emphases added). Thus, the plain and ordinary meaning of "independent" cannot be "different" as used here because such a change in meaning would contradict the very reason the applicant added the requirement of independent clocks.

Unable to avoid the applicant's reliance on "independent," the focus of Plaintiff's argument is additional arguments that the applicant made to distinguish the prior art. These additional arguments are irrelevant. As the Federal Circuit has explained, where the applicant "did assert multiple reasons for why [the prior art] is distinguishable, our precedent instructs that estoppel can attach to each argument." *Amgen Inc. v. Coherus Biosciences Inc.*, 931 F.3d 1154, 1159 (Fed. Cir. 2019). As shown above, the applicant used "independent" 11 times in explaining why the art was insufficient. "Independent"—not just sets—was, at a minimum, one of multiple reasons. *See* Dkt. 39-9 (Ex. H) at 11 (Applicant's Resp. (Nov. 29, 2012)) ("As discussed above, neither Jacobowitz nor Kim discloses having sets of processor cores ***configured to receive multiple and independent clock signal***."); *id.* at 10–11 (explaining the "***first clock signal is <u>independent</u> from the second clock signal"*** and "***[i]nstead,*** Kim discloses the apparatus comprising a multi-core processor (i.e., 100 in FIG. 1 or 200 in FIG. 2) having ***a <u>single</u> clock source***").

As to the additional arguments, first, Plaintiff points to other distinguishing arguments (multiple sets) that the applicant ***also*** made. Resp. at 5–6. Plaintiff is wrong "that neither Jacobowitz nor Kim teach 'sets of processor cores'" (Resp. at 6).[2] Second, Plaintiff argues that for

[2] As the Examiner found, Figure 6 of *Jacobowitz* discloses two sets of cores: "V0 cores 102 (top set)" and "V1 cores 102 (bottom set)." Dkt. 39-7 (Ex. F) at 4 (Office Action (Aug. 29, 2012)); *see also* Dkt. 39-5 (Ex. D) (*Jacobowitz*) at [0038] (stating that the "configuration of FIG. 6 may be employed in designs where ***multiple cores 102 are grouped*** in different regions of the [] chip").

Jacobowitz, "V_R was only a single signal," so "different" is sufficient. Resp. at 4. But even if correct, this does not change the fact that different is ***not*** sufficient to distinguish *Kim* or the *Jacobwitz-Kim* combination that applicant had to and did distinguish. Further, as to *Jacobowitz*, even if Plaintiff could have distinguished *Jacobowitz* by using the term "different," it did not. *See Tech Props. Ltd. LLC v. Huawei Techs. Co.*, 849 F.3d 1349, 1359 (Fed. Cir. 2017) (noting "the scope of surrender is not limited to what is absolutely necessary to avoid a prior art reference; patentees may surrender more than necessary" and "[w]hen this happens, we hold patentees to the actual arguments made, not the arguments that could have been made."). Third, Plaintiff conflates the issue by arguing that "the first and second clock signals of the original claim are not the same signals as in the disputed term." Resp. at 3–4. This is irrelevant. The Applicant specifically addressed the newly added claim language—"the first clock signal is independent from the second clock signal"—not the original claims that already stood rejected. Dkt. 39-9 (Ex. H) at 9–11.

Ultimately, Plaintiff's Response Brief presents no basis to ignore the applicant's ***eleven*** uses of "independent" to distinguish the prior art that confirm that "different" is not a plain and ordinary meaning of "independent" that works in this situation. While not necessary, those same prosecution history statements also meet the standard for a clear and unmistakable disavowal of claim scope. Accordingly, given the parties' clear dispute as to plain and ordinary meaning and consistent with the intrinsic record, the Court should find that the plain and ordinary meaning requires that the first and second clock signals are provided by or processed (i.e., divided or multiplied) from different reference oscillator clocks.

B. Term 2: "each processor core from the first/second set of processor cores is configured to dynamically receive a first/second supply voltage [from a power control block] and a first/second output clock signal"

This term is indefinite because the '339 Patent and the term fail to inform a POSITA, with reasonable certainty, of what it means for a processor core to be "configured to dynamically

receive" the recited signals. *See Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). Plaintiff contends this claim should be given its "plain and ordinary meaning," but fails to clarify the scope of such meaning in its Response Brief. *See* Resp. at 7–10. Based on its statements, Plaintiff appears to contend that configuring something to dynamically receive means that it simply receives a dynamic signal. *See id.* at 8 (contending this term "merely refers to the set of processor cores being configured to receive changing voltage and clock signals, such as for jobs with differing computational demands."). However, this contention does not reflect the language of the claim.

Plaintiff's arguments seek to read out the "configured to" language of this term. By reciting processor cores "***configured to*** dynamically receive" signals, the claim language requires that the process cores actually be configured in some way beyond mere reception of a voltage signal. A processor core that receives signals (dynamic or not) without needing any configuration cannot be said to be ***configured to dynamically receive***. This issue is at the core of the term's indefiniteness—the term does not inform a POSITA with reasonable certainty when a processor core is, or is not, configured to dynamically receive signals, and Plaintiff has not pointed to anything in the specification that could provide such guidance.

Instead, Plaintiff alleges that the Cheng paper (Dkt. 41-2 or "Cheng"), which is cited as prior art on the face of the '339 Patent, includes "one configuration that might allow a set of processor cores to dynamically receive a first supply voltage and a first output clock signal." Resp. at 8–9. First, the disclosures of Cheng are not incorporated into the specification itself, and the specification does not disclose any configuration of the processor cores that would allow a POSITA to understand what it means to dynamically receive signals. *See generally* '339 Patent. Second, Cheng was included in an Information Disclosure Statement filed with a Request for

Continued Examination on April 25, 2013, over three years ***after*** the '339 Patent was filed and after the asserted claims had already been allowed. Ex. 3 at 7 (Information Disclosure Statement (Apr. 25, 2013) disclosing Cheng); *see also id.* at 2 (Notice of Allowance (Feb. 14, 2013)). As is most often the case with such references disclosed by an applicant during patent prosecution, the applicant here was disclosing prior art that needed to be distinguished to show patentability, the opposite of what the Plaintiff relies upon Cheng for in this case. The applicant was not providing later-in-time supporting disclosure for the claims recited years before.

Third, and finally, Cheng's prior art disclosure does not resolve the indefiniteness of this term. Plaintiff fails to explain what aspect of its cited figure from Cheng relates to configuring processor cores to dynamically receive signals or how the proffered example could be paired with the distinct disclosure of the '339 Patent. Resp. at 9. In fact, the cited figure shows the processor core as a simple black box. Dkt. 41-2 at 1237–38, Fig. 4; *see also* Resp. at 9 (citing Cheng as disclosing "dynamic voltage and frequency ***scaling*** (DVFS)" not ***dynamic reception***). The cited image from Cheng provides no detail about what configuration of the core itself allows it to "dynamically receive" a signal. Dkt. 41-2 at 1238.

There is nothing within the '339 Patent, the cited Cheng reference, or the knowledge of a POSITA that informs with reasonable certainty what "necessary configurations" (Resp. at 10) are required to fall within the scope of this term. Therefore, this term is indefinite.

C. Term 3: "located in a periphery of the multi-core processor"

This term is indefinite because it fails to inform a POSITA, with reasonable certainty, when a component is "located in a periphery of the multi-core processor" and when it is not. *See Nautilus*, 572 U.S. at 901. Rather than clarify the scope of the purported plain and ordinary meaning of this term—including addressing whether a control block that is separated from the multi-core processor by some distance is nevertheless on the periphery—Plaintiff focuses on high-

level and simplified descriptions and illustrations of a single exemplary embodiment included in the specification. Resp. at 10–11; *see also Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1373–74 (Fed. Cir. 2014) ("With this lone example, a skilled artisan is still left to wonder what other forms of [the invention fall within the scope of the claim term]. … The specification offers no indication, thus leaving the skilled artisan to consult the 'unpredictable vagaries of any one person's opinion.'") (internal citations omitted). The '339 Patent's description of a multi-core processor does not account for practical considerations of processor architectures, including how a multi-core processor is arranged on a die and how a multi-core processor is packaged. *See* Villasenor Decl. at ¶¶ 75–77. These real-world complications go beyond the idealized description provided in the specification. Dr. Villasenor's opinion acknowledges the limitations and simplification present in the specification and does not "ignore[] the specification," as Plaintiff argues. Resp. at 12.

In particular, Figure 1 of the '339 Patent exemplifies the simplified nature of the specification—the processor cores and control blocks are illustrated as non-descript boxes and the interface circuit is illustrated as simple lines between the processor cores. In its Response Brief, Plaintiff focuses on one embodiment to contend the '339 Patent "clarifies the metes and bounds of the multi-core processor, placing the control blocks at its edges." Resp. at 11. Specifically, Figure 1 arranges the components of a multi-core processor for ease of illustration, and Plaintiff argues that the location of the control blocks in this Figure constitutes the periphery. However, while the periphery of this one simplified arrangement of components may be ascertained, that alone does not inform a POSITA with reasonable certainty as to the scope of this term; there are real-world arrangements of processor cores where a POSITA would not know whether a control block is located in a periphery of a multi-core processor or not. Villasenor Decl. at ¶¶ 81–83.

Plaintiff also modifies Dr. Villasenor's Figure C in a simplistic way that fails to address the indefiniteness of this term. Resp. at 12–13. As demonstrated in the Opening Brief and in Dr. Villasenor's declaration, many reasonable (i.e., not "unique and bizarre" (*id.* at 13)) architectures for multi-core processors highlight the difficulty in understanding this term's scope. Villasenor Decl. at Figures C, D, E. The simplistic exemplary multi-core processor in the '339 Patent fails to inform a POSITA of the bounds of "periphery" in this context, and thus the term is indefinite.[3]

D. Term 4: "located in a common region that is substantially central to the first set of processor cores and the second set of processor cores"

This term is indefinite because it fails to inform a POSITA, with reasonable certainty, both (1) when a component is "located in a common region," or not, and (2) when the "common region" is "substantially central," or not. *See Nautilus*, 572 U.S. at 901. With respect to "located in a common region," Plaintiff focuses on "region," a term that Defendant does not necessarily argue is indefinite, rather than the disputed term "common region." Resp. at 14–15. Plaintiff's arguments regarding "region," which are largely a red herring, are also inconsistent and do not address the core dispute here—when a region is "common" and when it is not. *Id.*[4]

Plaintiff also fails to provide clarification of the plain and ordinary meaning of "substantially central." Plaintiff contends that "all that is required is some standard for measuring the term of degree," but Plaintiff does not articulate ***any such*** standard for "measuring" when

[3] Plaintiff puts forth a strained analogy between the terms "outdoors" and "periphery" and argues that both terms "raise[] an edge case ***where the factual determination is difficult***." Resp. at 13. While there are other faults with this analogy, most glaringly, a POSITA would understand that an architecture where sets of cores are separate and not adjacent is not merely an "edge case." Villasenor Decl. at ¶ 81.

[4] Plaintiff focuses on claim differentiation (Resp. at 15), but Defendant's argument does not depend on claim differentiation, and this term is indefinite regardless of arguments on that issue.

something is "substantially central." Resp. at 16–17 (citing *Exmark Mfg. Co. Inc. v. Briggs & Stratton Power Prods. Grp., LLC*, 879 F.3d 1332, 1346 (Fed. Cir. 2018)).

To the extent that Plaintiff argues that the applicable "standard" is "not along the outside of the multi-core processor but the inside" (Resp. at 16), this is overbroad; a POSITA would still not be informed with reasonable certainty as to the scope of the term. While one configuration may fall within the term's bounds—e.g., directly in the middle of the multi-core processor's cores—"substantially central" remains indefinite with respect to numerous other real-world processor configurations. *See* Villasenor Decl. at ¶¶ 81–82, Figures C, D, E; *see also Interval Licensing*, 766 F.3d at 1373–74 ("With this lone example, a skilled artisan is still left to wonder what other forms of [the invention fall within the scope of the claim term]."). As explained in the Opening Brief and in Dr. Villasenor's declaration, a POSITA cannot determine with reasonable certainty the scope of each of "common region" and "substantially central," and this term is indefinite. Op. Br. at 16–20; Villasenor Decl. at ¶¶ 84–98.

III. CONCLUSION

Because only Defendant's claim construction positions properly account for the '339 Patent's file history and the understanding of a POSITA, they should be adopted.

Dated: January 22, 2025

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing document was served on counsel of record via the Court's electronic filing system on January 22, 2025.

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